at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring formed on said insulating film for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode wherein said wiring is connected to said one of the impurity regions through a hole opened in said insulating film;

a data line formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island;

a first interlayer insulating film formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line;

a voltage supply line formed on said first interlayer insulating film connected to one of the pair of impurity regions of the second semiconductor island;

an address line formed on said first interlayer insulating film connected to the first gate electrode wherein said address line extends across said data line;

a second interlayer insulating film formed over said first interlayer insulating film and said voltage supply line;

a pixel electrode formed over said second interlayer insulating film connected to the other one of the pair of the impurity regions of the second semiconductor island.

11. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

an insulating film formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring formed on said insulating film for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode wherein said wiring is connected to said one of the impurity regions through a hole opened in said insulating film;

a data line formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island;

a first interlayer insulating film formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line;

an address line formed on said first interlayer insulating film connected to the first gate electrode wherein said address line extends across said data line;

a surface smoothing film formed over said first interlayer insulating film and said address line;

a pixel electrode formed over said surface smoothing film connected to the other one of the pair of the impurity regions of the second semiconductor island.

Please add new claims 13-23 as follows:

13. A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor island, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode; and

a pixel electrode electrically connected to one of the pair of the impurity regions of the second semiconductor island;

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

14. The semiconductor device according to claim 13 wherein said first and second semiconductor islands comprise polysilicon.

15. The semiconductor device according to claim 13 further comprising a data line electrically connected to the other one of the impurity regions of the first semiconductor island.

16. A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

an interlayer insulating film formed over said wiring; and

a pixel electrode formed over said interlayer insulating film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

17. The semiconductor device according to claim 16 wherein said first and second semiconductor islands comprise polysilicon.

18. The semiconductor device according to claim 16 further comprising a data line electrically connected to the other one of the impurity regions of the first semiconductor island.

19. The semiconductor device according to claim 16 wherein said wiring is located below the interlayer insulating film.

20. A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

a surface smoothing film formed over said wiring; and

a pixel electrode formed over said surface smoothing film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

21. The semiconductor device according to claim 20 wherein said first and second semiconductor islands comprise polysilicon.

22. The semiconductor device according to claim 21 further comprising a data line electrically connected to the other one of the impurity regions of the first semiconductor island.